	Type	L #	Hits	Search Text	DBs
1	BRS	L1	24	tu near kuo-chi.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	220	438/25.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	125885	(non-volatile) near35 (volatile)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	65444	(non-volatile near memory) near35 (volatile near memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L5	324	(non-volatile near memory near region) near35 (volatile near memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	1427	((non-volatile near memory) near35 (volatile near memory)) near35 (electrode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L7	0	((non-volatile near memory) near35 (volatile near memory)) near35 (electrode) near35 (poly-oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L8	0	((non-volatile near memory) near35 (volatile near memory)) near35 (electrode) near35 (poly near oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L9	0	((non-volatile near memory) near35 (volatile near memory)) near35 (electrode) near35 (polyoxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
					US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L11	7388	(poly near oxide)	
11	BRS	L12	1100	(polyoxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
12	BRS	L10	202	(poly-oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
13	BRS	L13	8	(poly-oxide) near15 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
14	BRS	L14	12	(polyoxide) near15 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
15	BRS	L15	70	(poly near oxide) near15 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
16	BRS	L16	70	(poly near oxide or poly-oxide or poly-oxide) near15 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
17	BRS	L17	7388	(poly near oxide or poly-oxide or poly-oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
					US-PGPUB; USPAT;
18	BRS	L18	8313	(poly near oxide or polyoxide or poly-oxide)	EPO; JPO; DERWENT; IBM_TDB
19	BRS	L19	8313	((poly near oxide) or (polyoxide) or (poly-oxide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
20	BRS	L20	82	((poly near oxide) or (polyoxide) or (poly-oxide)) near15 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
21	BRS	L21	0	((poly near oxide) or (polyoxide) or (poly-oxide)) near15 (split-gate near transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
22	BRS	L22	0	(non-volatile near memory near region) near35 (volatile near memory) near25 (poly-oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
23	BRS	L23	3	(non-volatile near memory near region) near35 (volatile near memory) near25 (poly near oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
24	BRS	L24	0	(non-volatile near memory near region) near35 (volatile near memory) near25 (polyoxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 6461984 B1	Semiconductor device using N2O plasma oxide and a method of fabricating the same
2			US 6246612 B1	Methods of erasing a memory device and a method of programming a memory device for low-voltage and low-power applications
3			US 6238983 B1	Alignment dip back oxide and code implant through poly to approach the depletion mode device character
4			US 6144586 A	Methods of erasing a memory device and a method of programming a memory device for low-voltage and low-power applications
5			US 6058043 A	Method of erasing a memory device and a method of programming a memory device for low-voltage and low-power applications
6			US 5933748 A	Shallow trench isolation process

	U	1	Document ID	Title
7			US 5481128 A	Structure for flash memory cell
8			US 5444003 A	Method and structure for creating a self-aligned bicmos-compatible bipolar transistor with a laterally graded emitter structure
9			US 4898835 A	Single mask totally self-aligned power MOSFET cell fabrication process
10			US 4441249 A	Semiconductor integrated circuit capacitor
11			US 6238983 B	Provision of code implant for read-only memory involves combining alignment dip back procedure with double charge implant process
12			US 4898835 A	Multicell power MOSFET mfr. - using single mask, fully self-aligned process on a oxide-poly:silicon-poly-oxide structure